

FIG. 1

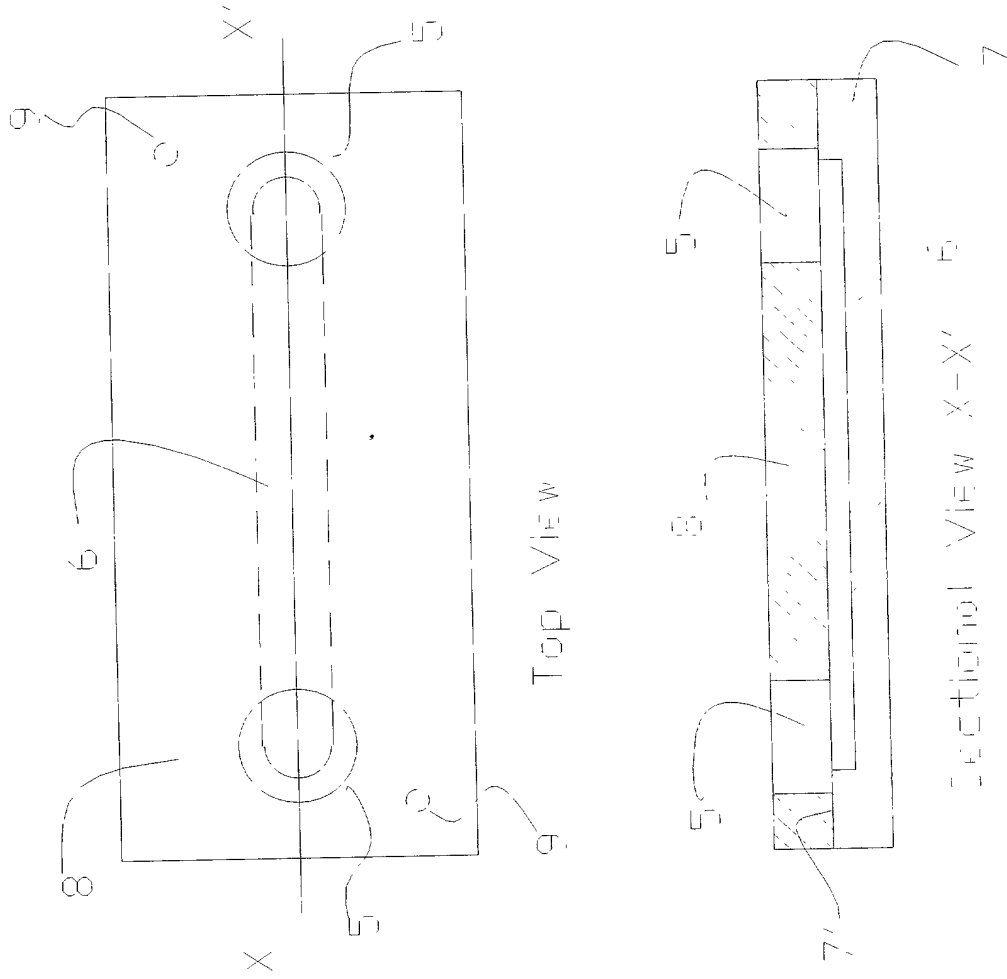


FIG. 2

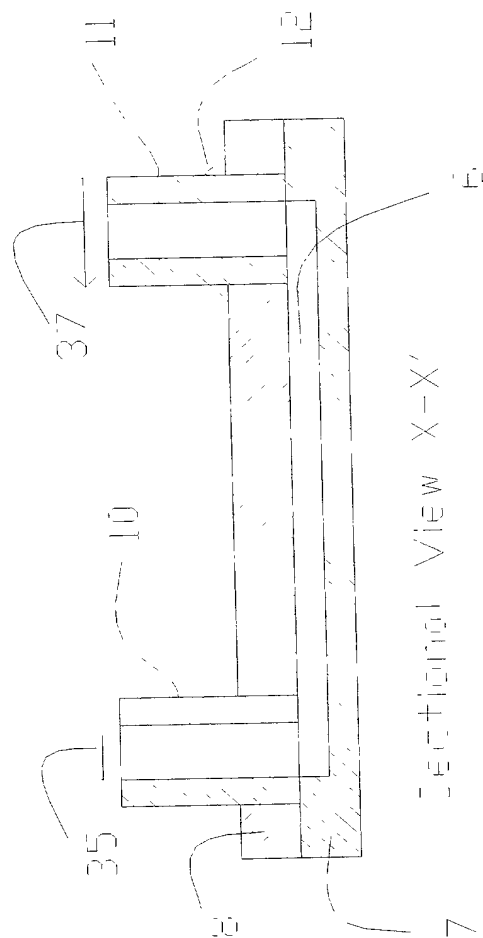
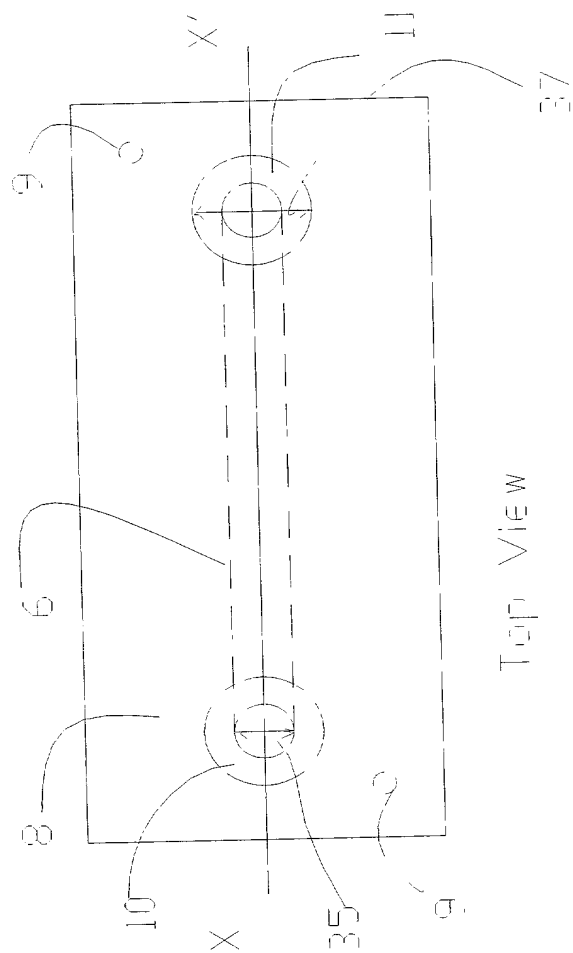


FIG. 3

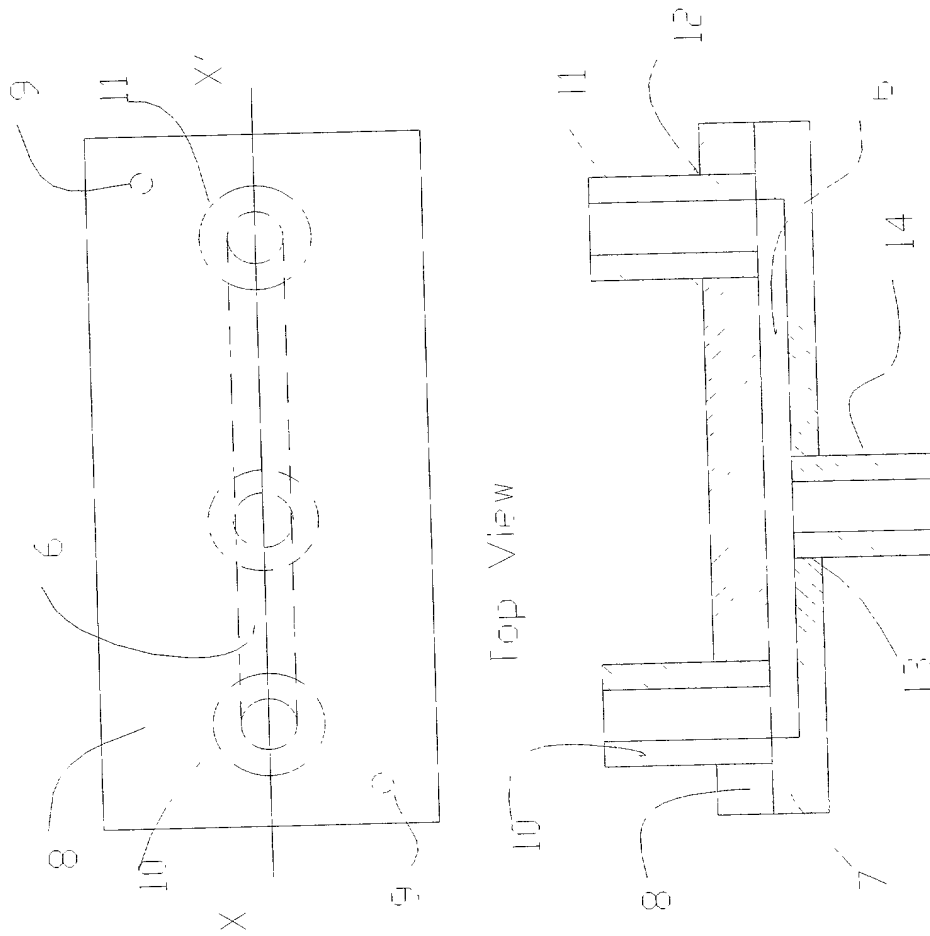


FIG. 4

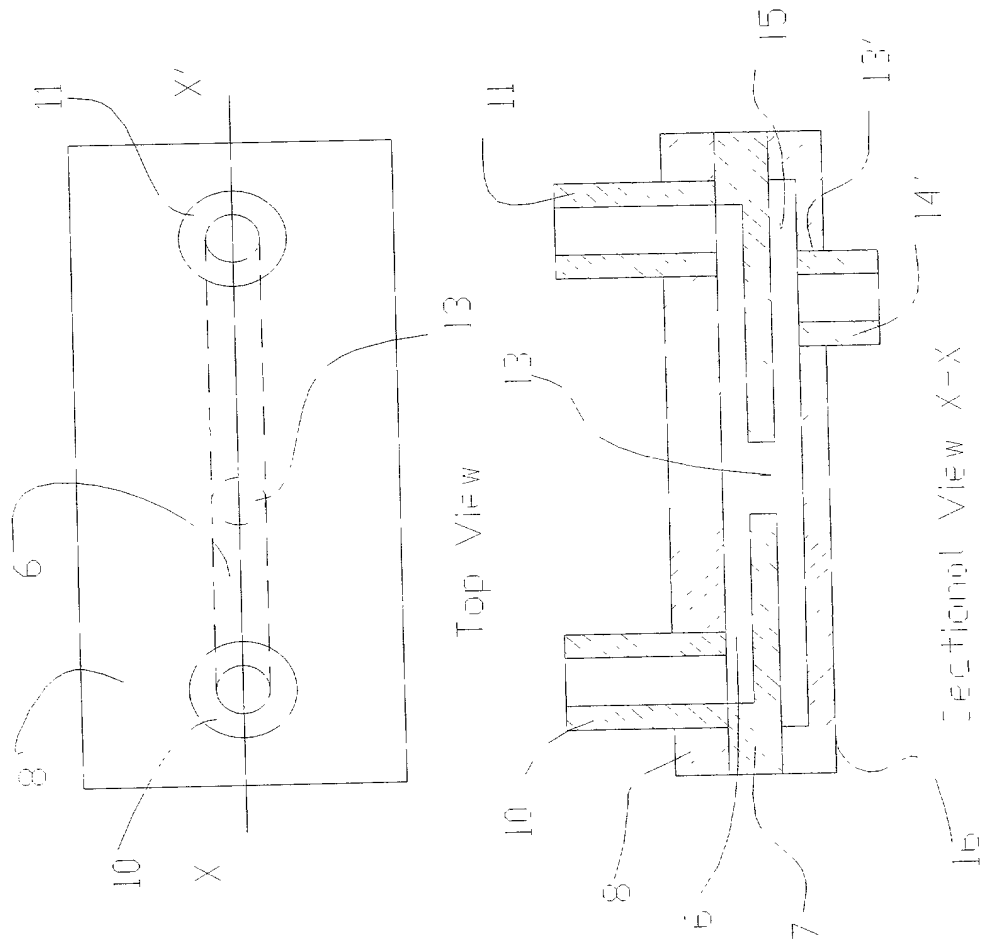


FIG. 5

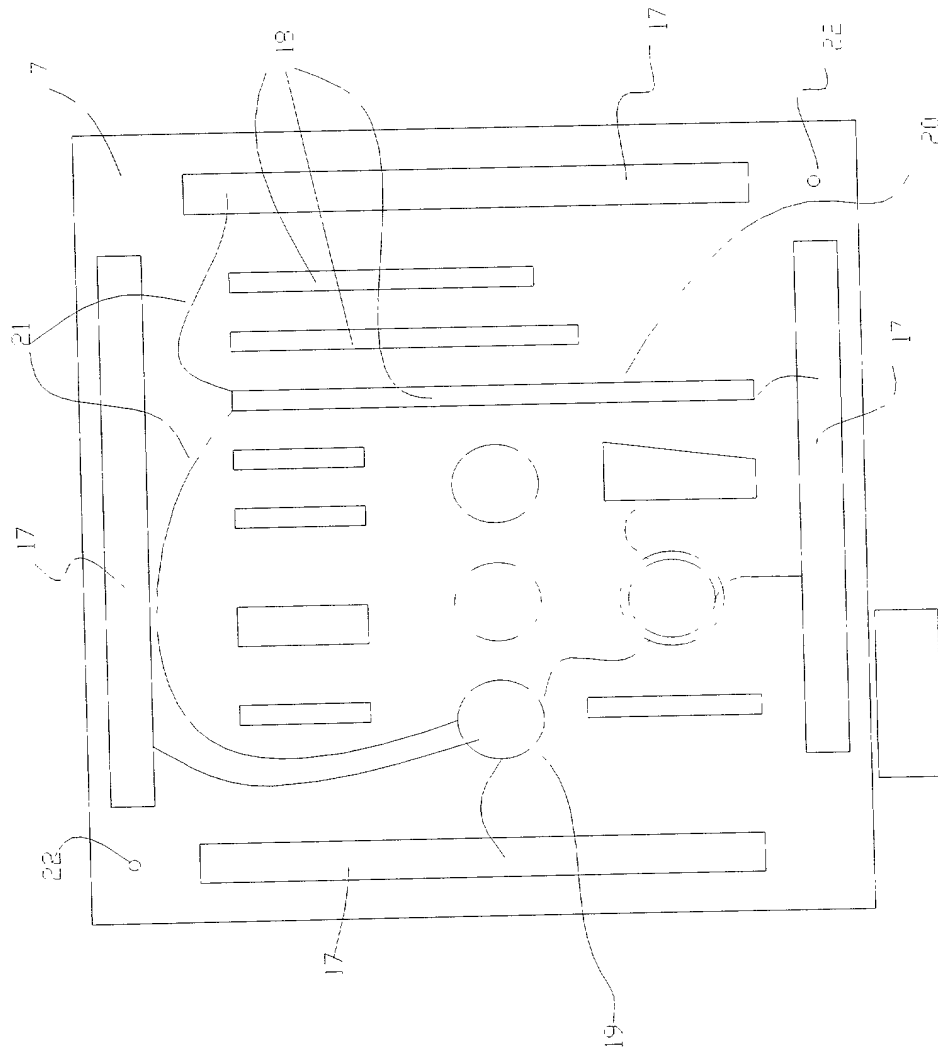


FIG. 6

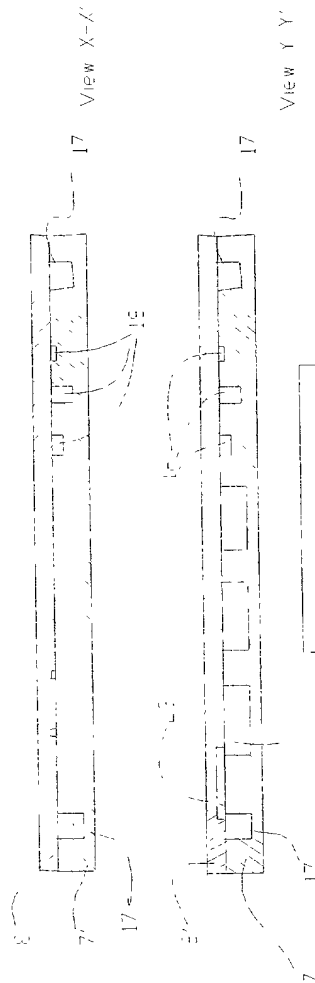
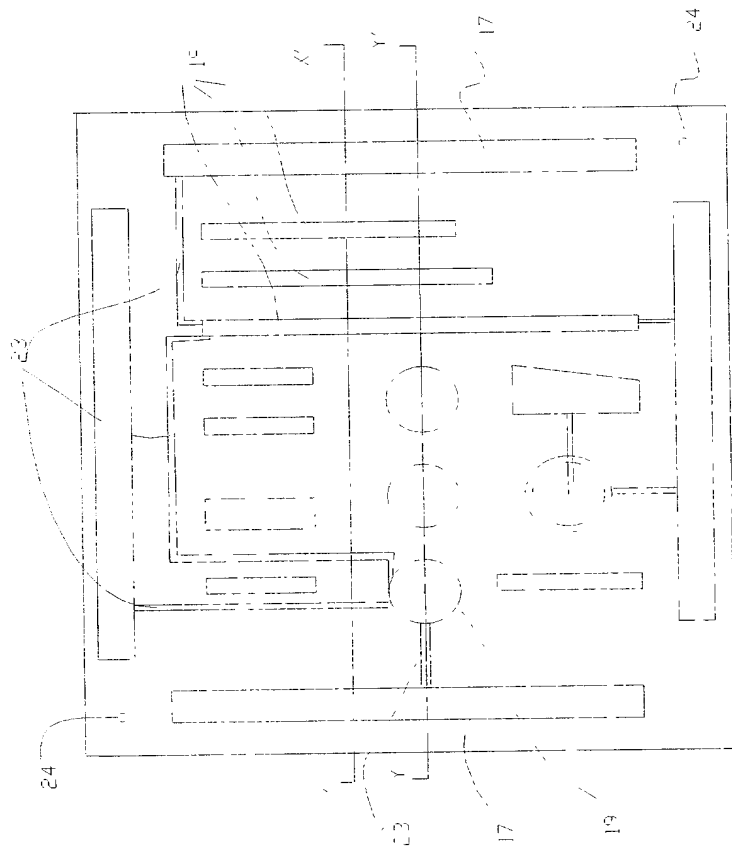


FIG. 7

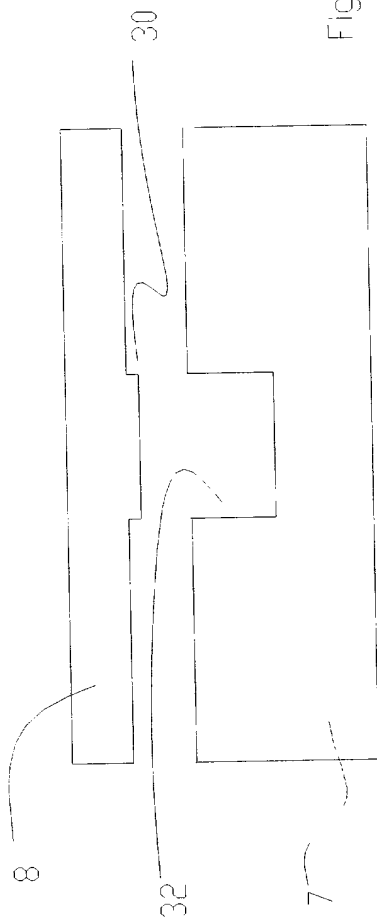


Figure 8A

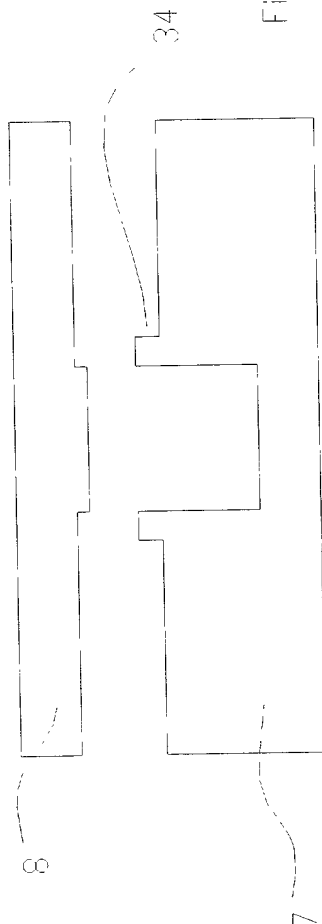


Figure 8B

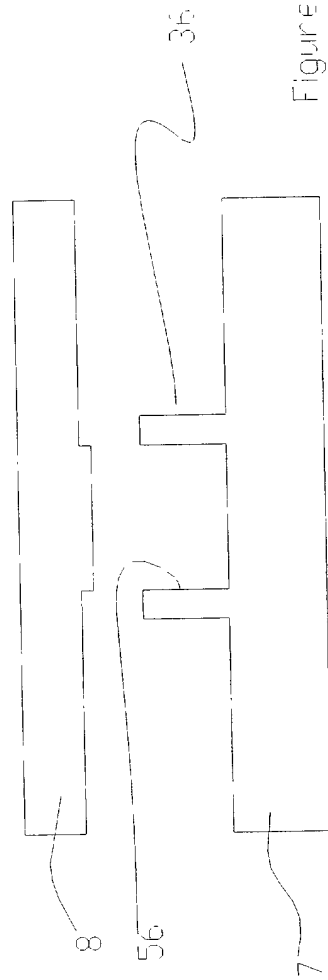


Figure 8C

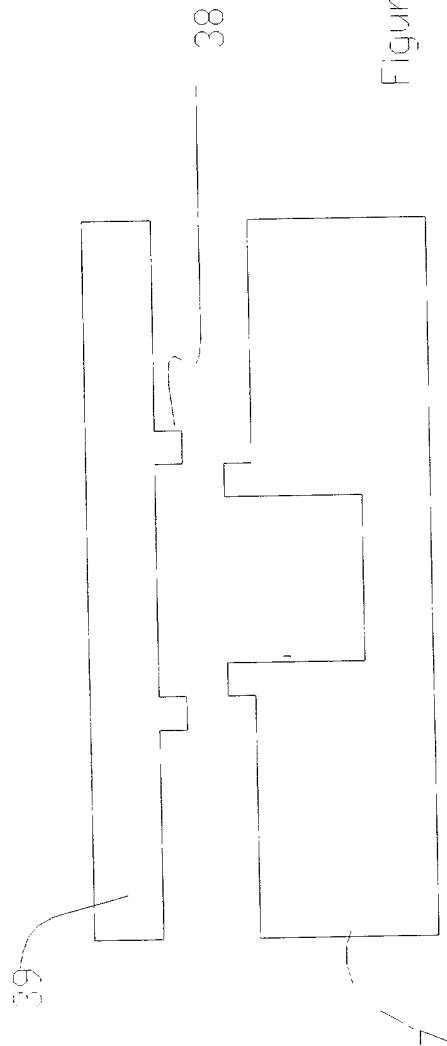


Figure 9A

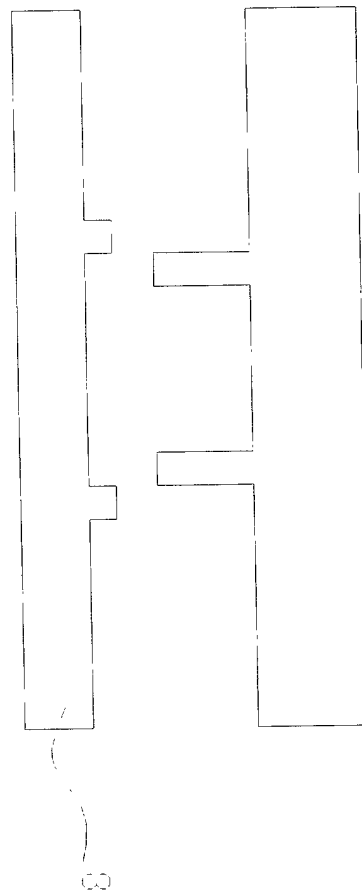


Figure 9B

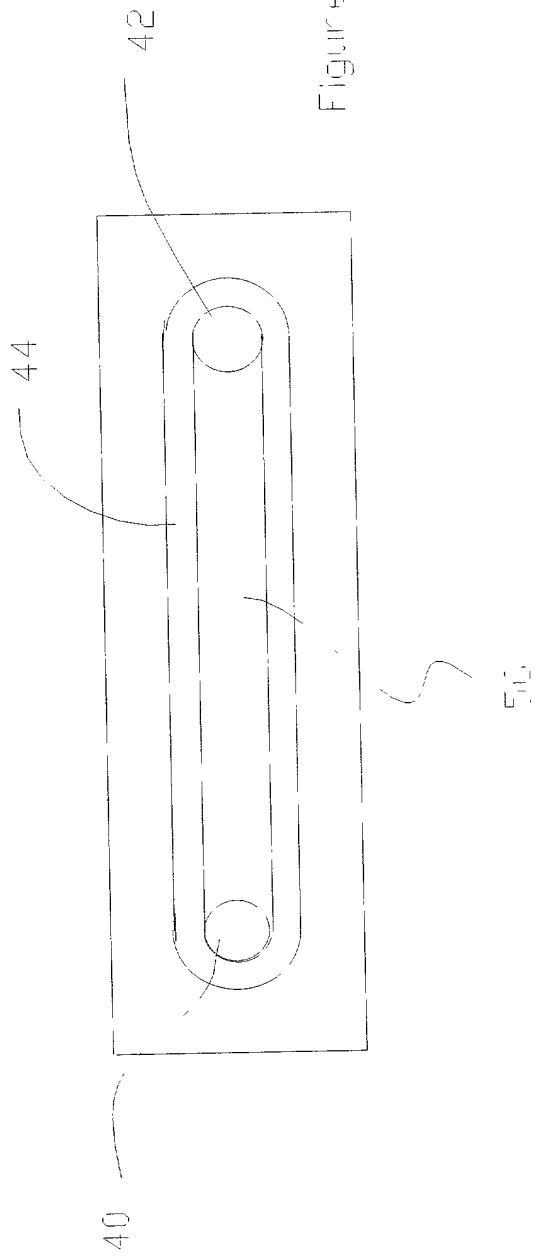


Figure 10A

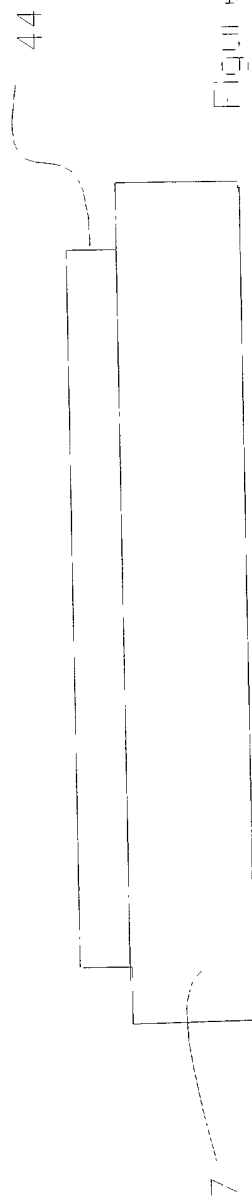
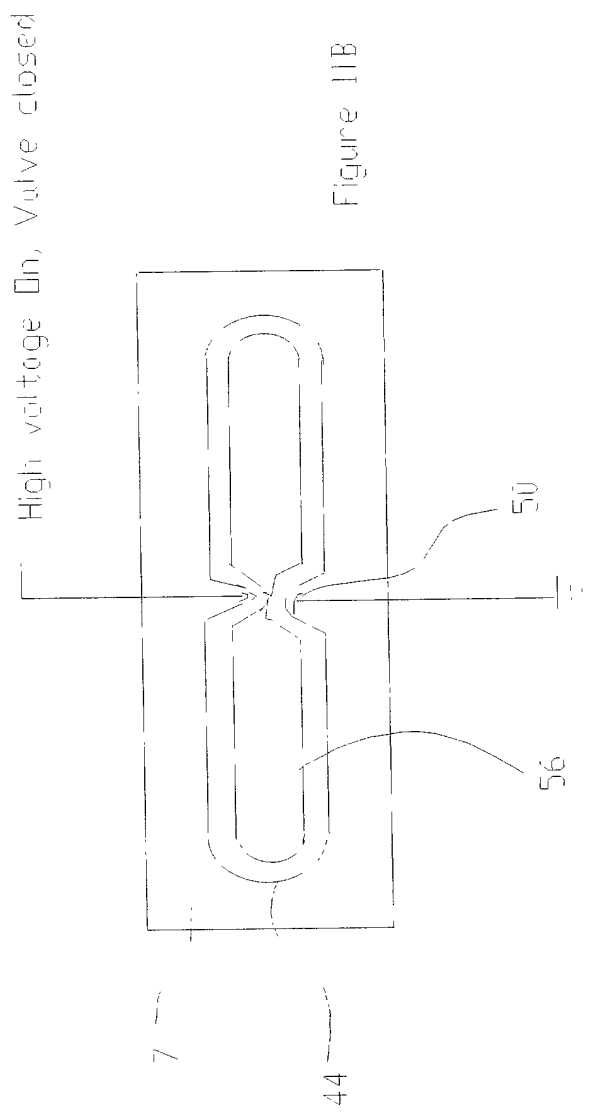
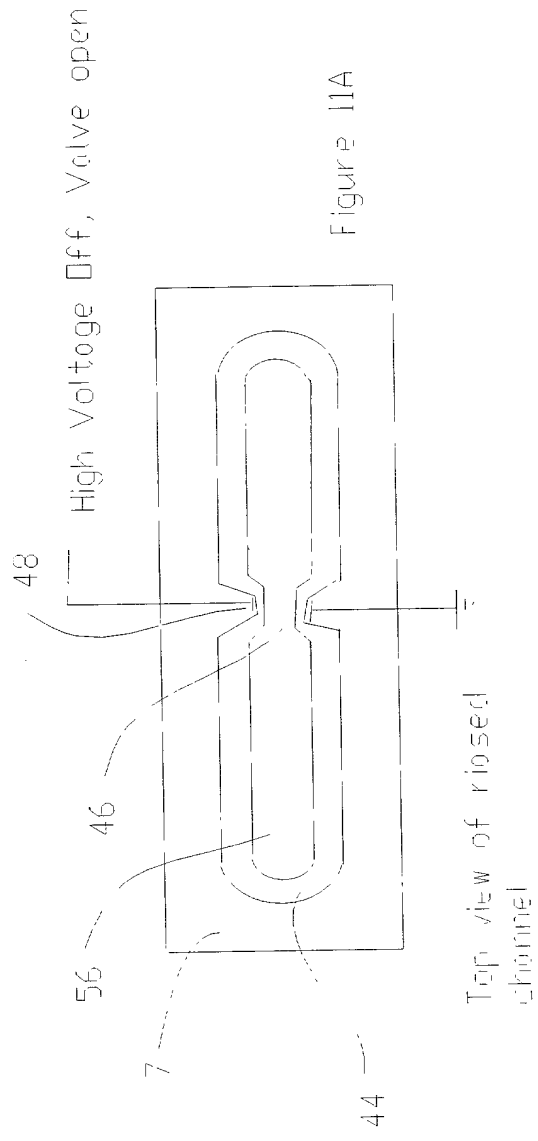


Figure 10E



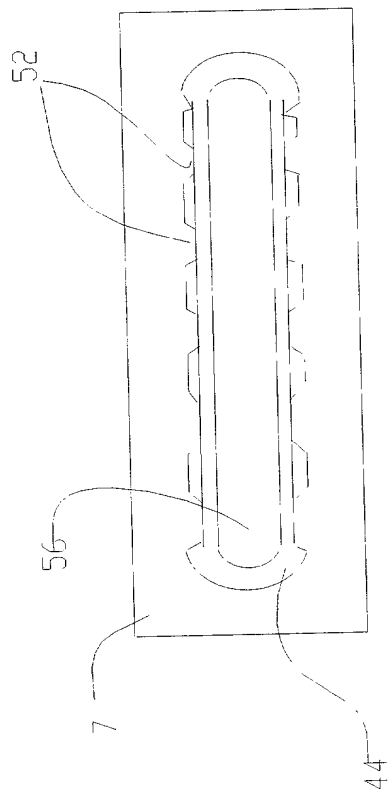


Figure 12A
Top View

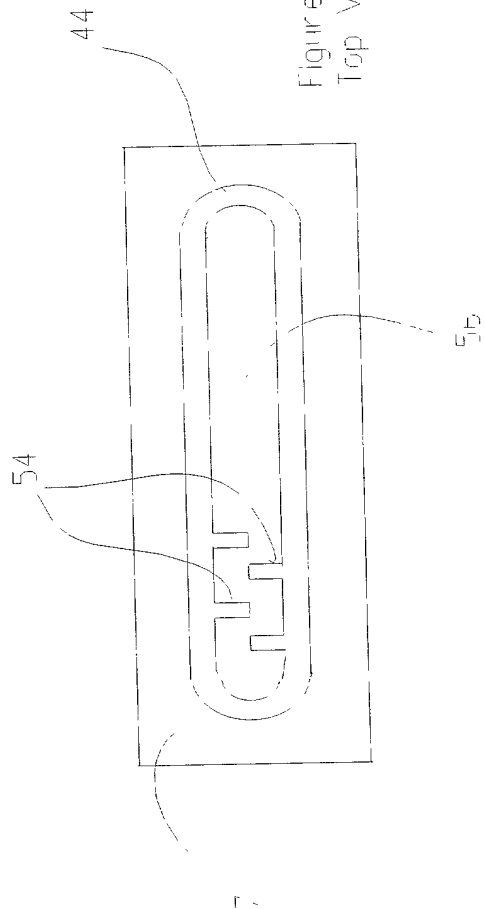


Figure 12B
Top View

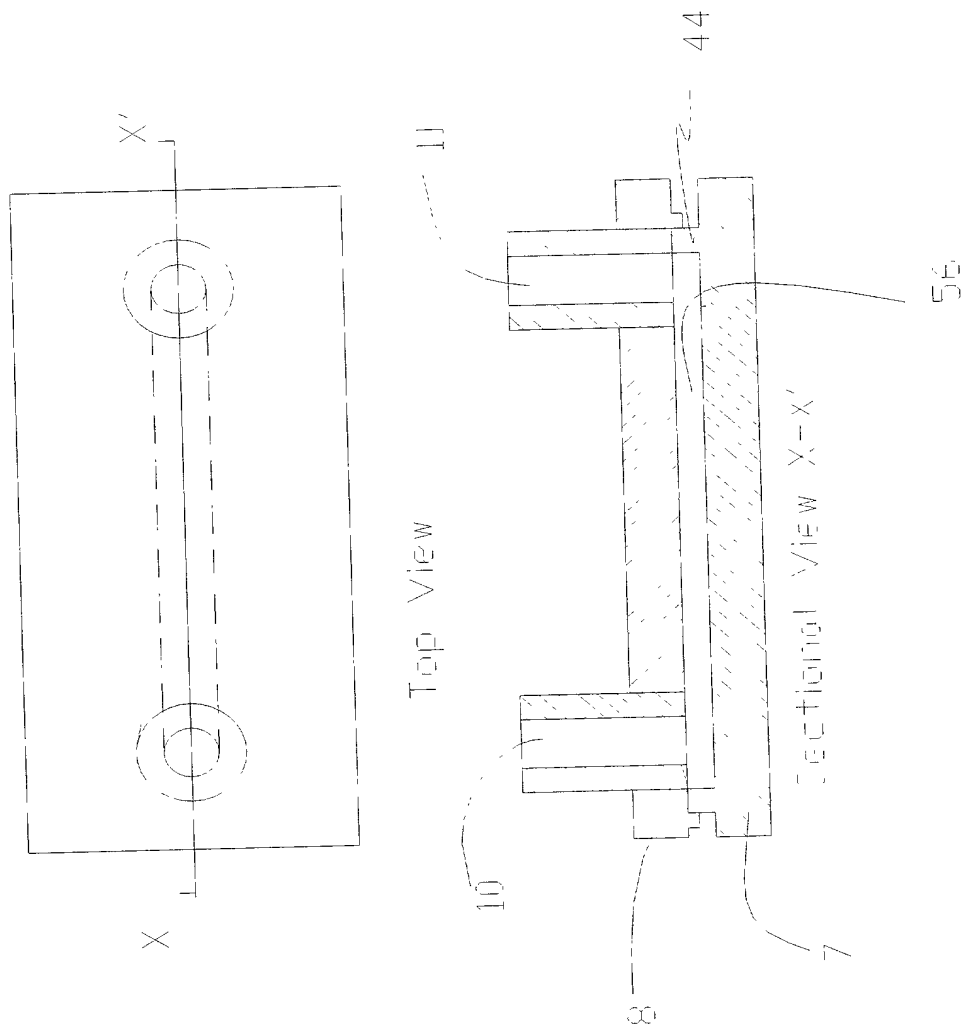
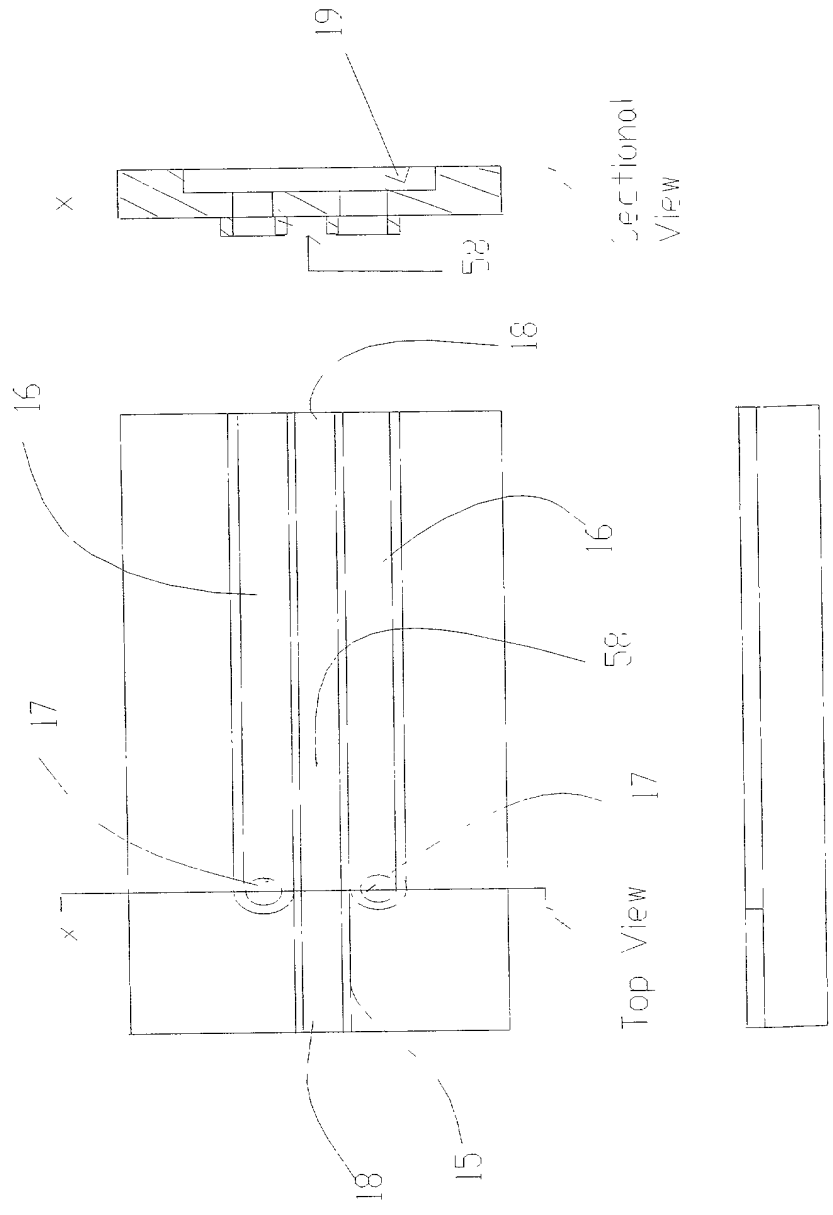


Figure 13



Side View

Figure 14

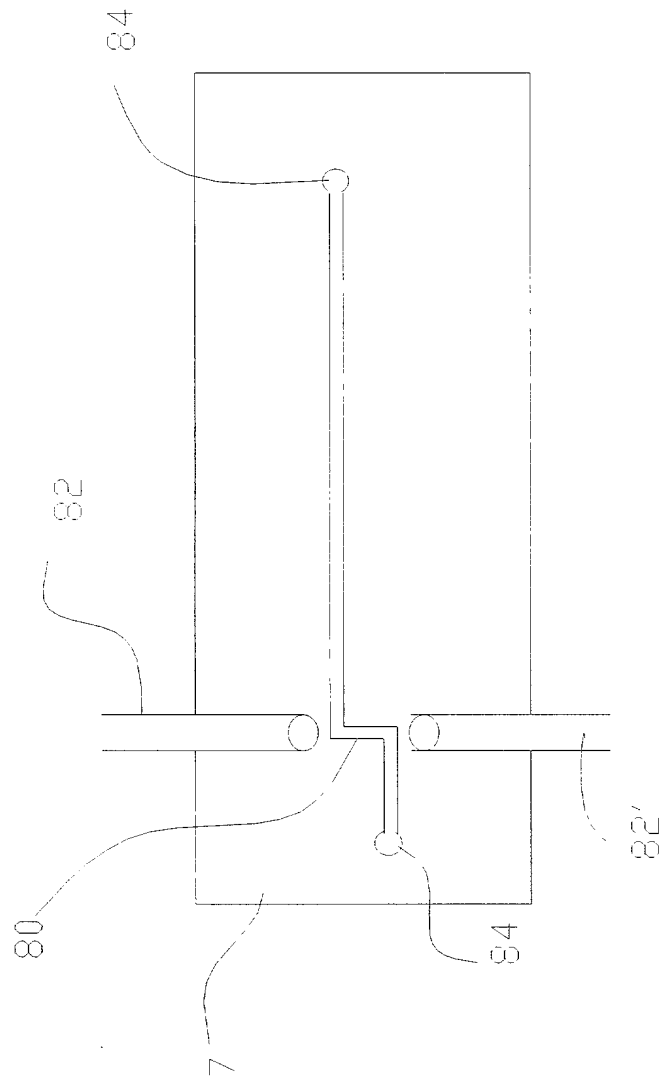


Figure 15A: Top view: Substrate without cover

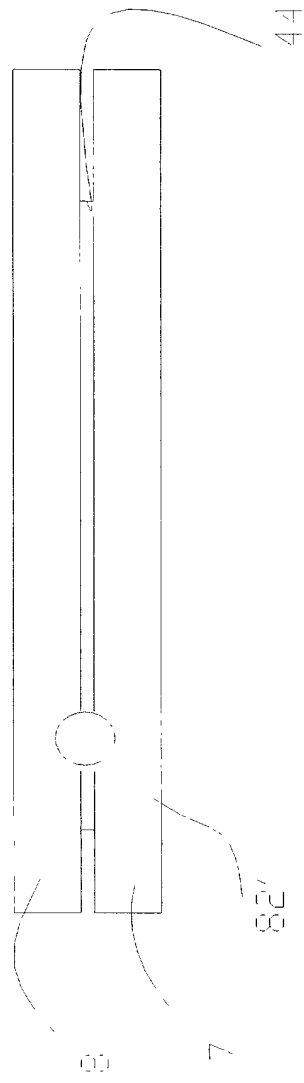


Figure 15B: Side view of assembled device

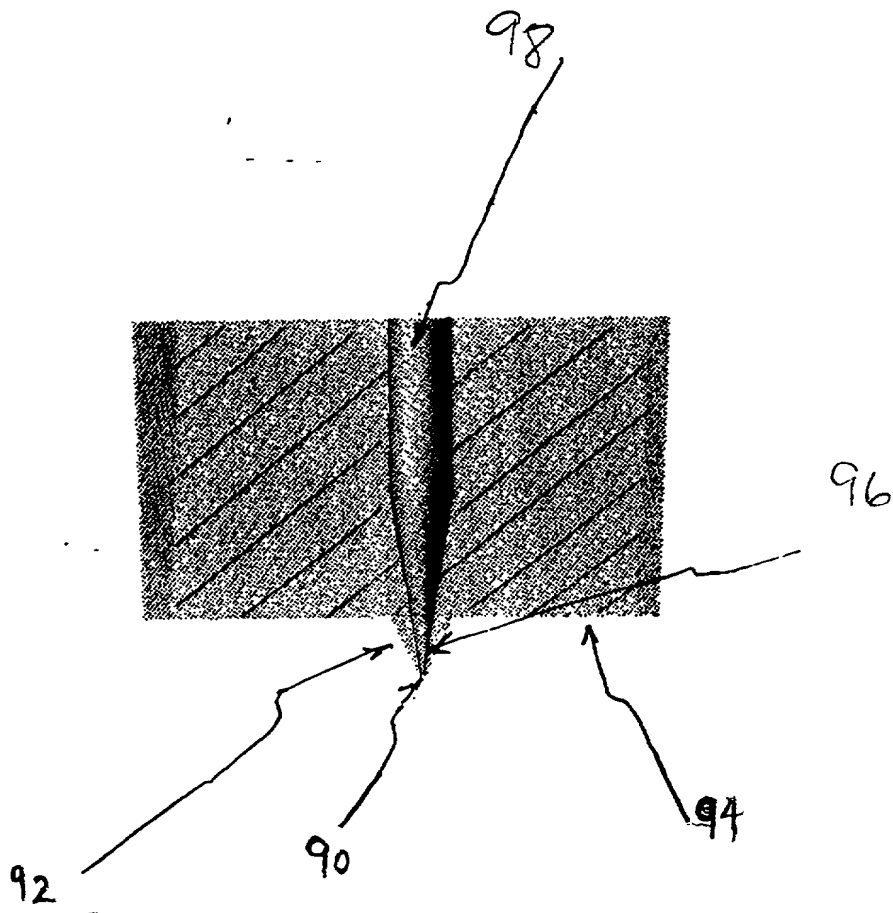


Figure 16

Figure 17

